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Current Position

Research Scholar and PhD Student in the Reconfigurable Architectures group of INRIA[1]/IRISA [2], Lannion, France, from Sep. 2009. (Research Area: Ultra-Low Power Design of Wireless Sensor Network Nodes) [Expected date of completion: October 2012]

Educational Qualifications

1. Master of Technology, Indian Institute of Technology Kanpur, India (2001), [Electrical Engineering, Microelectronics and VLSI]. *Grade:* 8.29/10.
2. Bachelor of Engineering, University of Mysore, India (1998), [Electronics and Communications]. *Grade:* 80% with 6th Rank [Top 2%]

Professional Experience

1. Marvell India Pvt. Ltd., Bangalore, India (Dec. 2006 - Mar. 2009) as Senior Design Engineer.
2. Philips (NXP) Semiconductors, Bangalore (Jan. 2006 - Dec. 2006) as Technical Leader.
3. C2Silicon Software Solutions, Bangalore (May 2004 - Dec. 2005) as Senior Member, Technical Staff.
4. Sanyo LSI Technology India Pvt. Ltd., Bangalore (May 2001 - Apr. 2004) as Design Engineer and Senior Engineer.

Publications

1. Vivek D. Tovinakere, Olivier Sentieys and Steven Derrien, "A Polynomial Based Approach to Wakeup Time and Energy Estimation in Power-Gated Logic Clusters," *Journal of Low Power Electronics*, vol. 7, no. 4, pp. 482-489, Dec. 2011.
2. Divya Krishna Murthy, Shen Li, Satoshi Goto, Tomoyashi Sato and Vivek T.D., "Dynamic Reconfiguration in Motion Estimation," in *Proc. ASP Intl. Conf. Embedded SoCs*, July 6-7, 2005, Bangalore, India.

Academic Honours

1. Placed in top 4% of candidates in Graduate Aptitude Test in Engineering (GATE), a national qualifying examination for postgraduate courses in technology in India (1998).
2. Secured scholarship for two years in Pre-University College for having been placed in top 2% and qualified in preliminary exams of National Talent Search Examinations (NTSE) of India (1992-1994).
3. Secured top honours [placed in top 2% of candidates] in Bachelor of Engineering (1998), Pre-University College (1994) and High School (1992).

[1] The French National Institute of Research in Computer Science and Automation
[2] Institute of Research in Computer Science and Random Systems

Skills

1. IC Design and Simulation Tools: Design Compiler, Formality, PrimeTime-PX/SI, Virtuoso, SoCEncounter, Circuit Simulators (Eldo, Spectre ADE), HDL and Netlist Simulators (ModelSim, NCVerilog, Verdi, VCS)
2. HDLs, Programming and Scripting Languages: Verilog, C, Perl, Tcl
3. Modeling Tools: MATLAB

Current Research

A key constraint in the design of computational nodes for Wireless Sensor Networks is their energy consumption. The nodes require very high degree of autonomy in their operation for extended lifetimes. With the scaling of MOS devices to nanoscale dimensions (90nm and below), the contribution of leakage current to total energy consumption has become significant, sometimes exceeding dynamic power consumption. This phenomenon is particularly important in the context of WSNs as nodes tend to remain in standby states for significantly long periods of time than in active states. In this work, we examine scalable architectures for reconfigurable finite state machines with ultra-low power consumption suitable for WSN nodes using *Power Gating*, with explorations at architecture and circuit levels. It involves an extensive study of design issues in power gating and modeling of design parameters at circuit level - of both combinational and sequential types. In particular, implementations of power-gated logic clusters and FSMs that are optimal in the sense of energy consumption will be investigated. It is also proposed to develop a design methodology to generate reconfigurable FSMs.

Summary of Activities

1. Gate-level power estimation, compact models for design parameters in power-gated circuits. Circuit level simulation of logic circuits in sub-100nm technologies.
2. Exploration of power-gating opportunities in reconfigurable logic circuits used in Wireless sensor network nodes; applicability in heterogenous FPGA architectures.
3. Design methodology for power-gated circuits (Variations to standard IC design flows)
4. Design of experimental circuits for understanding 3D-IC technologies and standard-cell development (Initial Phase)

Summary of Professional Experience

I have 8 years of experience in semiconductor and consumer electronics industry in various roles. A summary of my tasks and responsibilities at organizations I have worked for is provided below (in reverse chronological order).

1. *Implementation of an embedded processor subsystem in an ASIC for video devices*
   Defined architecture and designed a CPU sub-system (4M gates, 65nm CMOS technology) for a SoC. Held responsibility for logic synthesis, timing closure and formal verification for design sign-off with additional focus on optimization for leakage power and congestion. Other responsibilities included FPGA validation of sub-system core, design of peripheral interfaces and bring-up of CPU sub-system related design features during post-Silicon debug.
2. *Full chip verification of a multimedia applications processor for mobile phones*
   Developed directed tests for functionality checks at chip level for an ASIC based on Nexperia SoC platform of NXP, a product targeted for use in mobile phones.

3. *Architectures for Motion Estimation on a Dynamically Reconfigurable Processor*
   Designed parallel architectures for Full Search and Three-Step Search algorithms for Motion Estimation in a Video Encoder on a Dynamically Reconfigurable Processor; held responsibility for its implementation by the team.

4. *Algorithm and Architecture Modeling for Adaptive Equalizers in a PRML System*
   Modeled a Partial Response-Maximum Likelihood (PRML) symbol detection system for an ASIC targeted for Digital Video Cassette player. Validated algorithms used in signal processing datapath and evaluated performance of an adaptive equalizer before hardware design. Designed an adaptive equalizer to minimize ISI due to Read-Channel impairments of Magnetic Tape.

5. *Modeling DVB-S System for Evaluation of Blind Channel Equalization Algorithms*
   Modeled DVB-S Tx/Rx system in MATLAB to validate algorithms used in DVB-S receiver IC. It included modeling a DVB-S link and Phase Noise to evaluate receiver performance. Investigated Blind Channel Equalization algorithms for reducing ISI over DVB-S link.

6. *FFT Generator*
   Developed automated RTL generator (RTL in Verilog) for a fixed-point architecture of FFT intended for an OFDM application(DVB-T). Different lengths (4 to 8192) of FFT were supported for datapath widths 8 to 16. This also included a high-speed multiplier generation engine based on Modified Booth algorithm to support different datapath widths. Generated multipliers were used for synthesis with $0.35\mu m$ CMOS technology library.

Personal Information

1. Date of Birth: 24th June 1976
2. Nationality: Indian
3. Marital Status: Married
4. Language Skills: Fluent in English and two Indian Languages: Hindi and Kannada.
   Basic conversation skills in French.

References

Available on Request